FIG.1

DESCRIPTION OF 4-BIT GRAY CODE

DECIMAL CODE	BINARY CODE ADR<3~0>				GRAY CODE GADR<3~0>			
	<3>	<2>	<1>	<0>	<3>	<2>	<1>	<0>
	●	●	●	●				
0	0	0	0	0	0	0	0	0
				●				●
1	0	0	0	1	0	0	0	1
			●	●			●	
2	0	0	1	0	0	0	1	1
				●				●
3	0	0	1	1	0	0	1	0
		●	●	●		●		
4	0	1	0	0	0	1	1	0
				●				●
5	0	1	0	1	0	1	1	1
			●	●			●	
6	0	1	1	0	0	1	0	1
				●				●
7	0	1	1	1	0	1	0	0
	●	●	●	●	●			
8	1	0	0	0	1	1	0	0
				●				●
9	1	0	0	1	1	1	0	1
			●	●			●	
10	1	0	1	0	1	1	1	1
				●				●
11	1	0	1	1	1	1	1	0
		●	●	●		●		
12	1	1	0	0	1	0	1	0
				●				●
13	1	1	0	1	1	0	1	1
			●	●			●	
14	1	1	1	0	1	0	0	1
				●				●
15	1	1	1	1	1	0	0	0
	●	●	●	●				

● CARRY

↑ DOWNWARD DIRECTION

↓ UPWARD DIRECTION

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FIG.2

EXPRESSION CONVERTING 4-BIT GRAY CODE INTO 4-BIT BINARY CODE

BINARY CODE ADR<3~0>		GRAY CODE GADR<3~0>
ADR<3>	=	GADR<3>
ADR<2>	=	Exor(GADR<3>,GADR<2>)
ADR<1>	=	Exor(GADR<3>~GADR<1>)
ADR<0>	=	Exor(GADR<3>~GADR<0>)

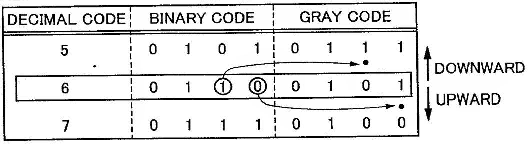
FIG.3

EXPRESSION CONVERTING N-BIT GRAY CODE INTO N-BIT BINARY CODE

BINARY CODE ADR<n-1~0>		GRAY CODE GADR<n-1~0>
ADR<n-1>	=	GADR<n-1>
ADR<n-2>	=	Exor(GADR<n-1>,GADR<n-2>)
ADR<n-3>	=	Exor(GADR<n-1>~GADR<n-3>)
⋮	⋮	⋮
ADR<0>	=	Exor(GADR<n-1>~GADR<0>)

FIG.4

EXEMPLARY LOCATION OF CARRY OF 4-BIT GRAY CODE



DECIMAL CODE	BINARY CODE				GRAY CODE			
5	0	1	0	1	0	1	1	1
6	0	1	①	⓪	0	1	0	1
7	0	1	1	1	0	1	0	0

FIG.5

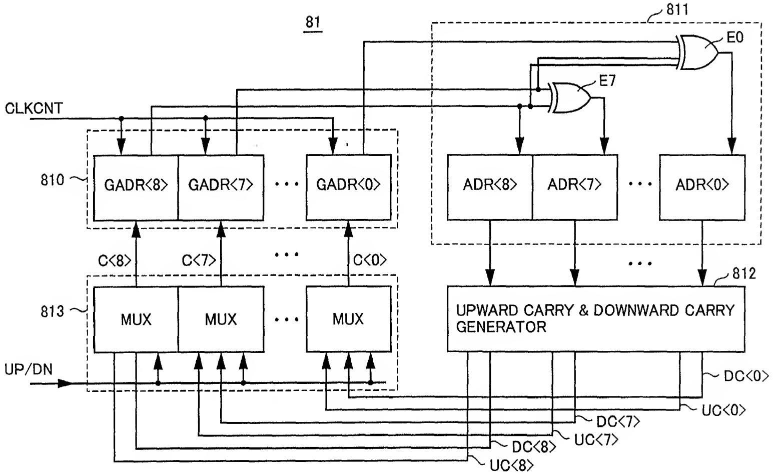

81
811
E0
E7
CLKCNT
810
GADR<8>
GADR<7>
GADR<0>
ADR<8>
ADR<7>
ADR<0>
C<8>
C<7>
C<0>
812
813
MUX
MUX
MUX
UPWARD CARRY & DOWNWARD CARRY GENERATOR
UP/DN
DC<0>
UC<0>
DC<7>
UC<7>
DC<8>
UC<8>

FIG.6

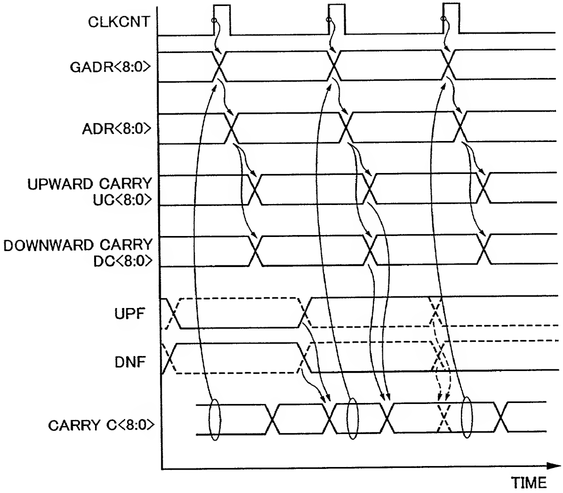

CLKCNT
GADR<8:0>
ADR<8:0>
UPWARD CARRY
UC<8:0>
DOWNWARD CARRY
DC<8:0>
UPF
DNF
CARRY C<8:0>
TIME

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FIG.7

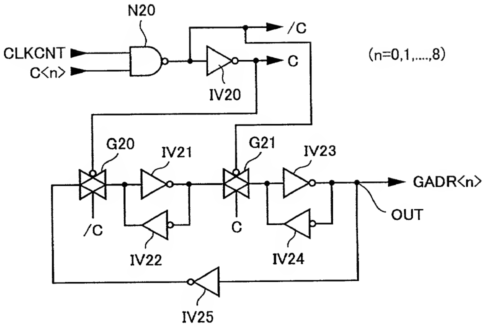

N20
/C
CLKCNT
C<n>
C
IV20
(n=0,1,....,8)
G20
IV21
G21
IV23
GADR<n>
OUT
/C
C
IV22
IV24
IV25

FIG.8

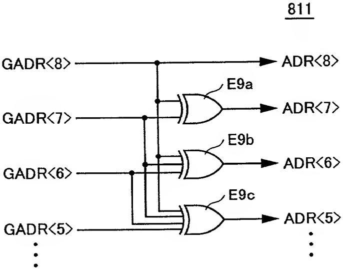

811
GADR<8>
ADR<8>
E9a
GADR<7>
ADR<7>
E9b
GADR<6>
ADR<6>
E9c
GADR<5>
ADR<5>

FIG.9

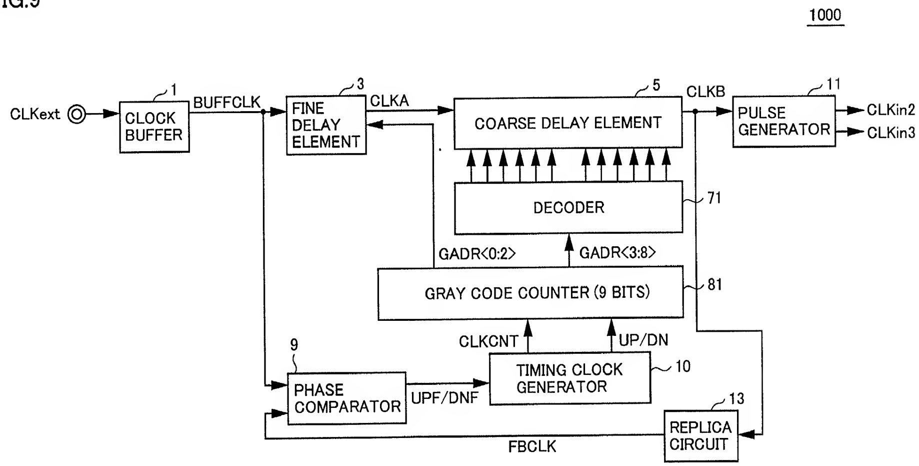
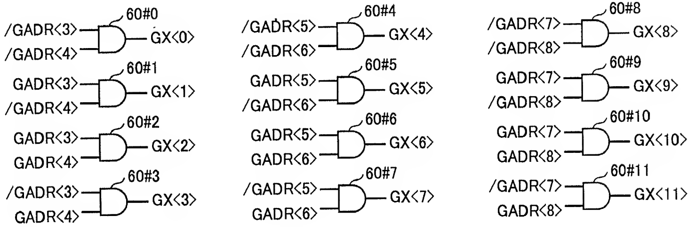
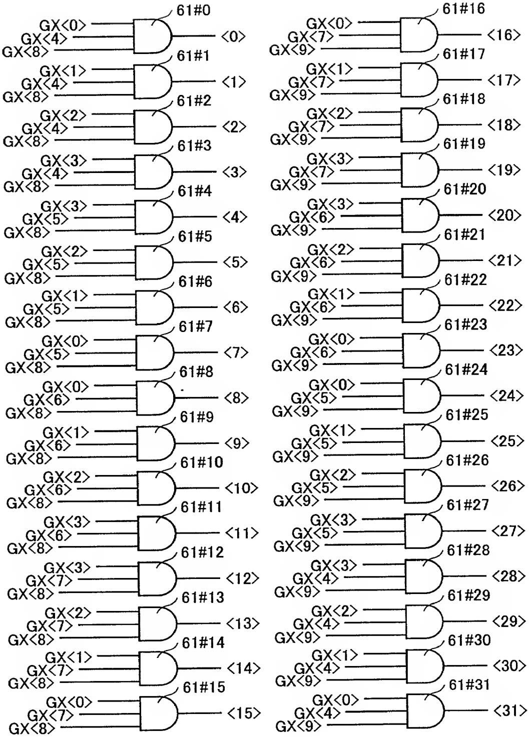

1000
CLKext
1
CLOCK BUFFER
BUFFCLK
3
FINE DELAY ELEMENT
CLKA
5
COARSE DELAY ELEMENT
CLKB
11
PULSE GENERATOR
CLKin2
CLKin3
DECODER
71
GADR<0:2>
GADR<3:8>
GRAY CODE COUNTER (9 BITS)
81
CLKCNT
UP/DN
9
PHASE COMPARATOR
UPF/DNF
TIMING CLOCK GENERATOR
10
13
REPLICA CIRCUIT
FBCLK

FIG.10



60#0
/GADR<3>
/GADR<4>
GX<0>
60#1
GADR<3>
/GADR<4>
GX<1>
60#2
GADR<3>
GADR<4>
GX<2>
60#3
/GADR<3>
GADR<4>
GX<3>
60#4
/GADR<5>
/GADR<6>
GX<4>
60#5
GADR<5>
/GADR<6>
GX<5>
60#6
GADR<5>
GADR<6>
GX<6>
60#7
/GADR<5>
GADR<6>
GX<7>
60#8
/GADR<7>
/GADR<8>
GX<8>
60#9
GADR<7>
/GADR<8>
GX<9>
60#10
GADR<7>
GADR<8>
GX<10>
60#11
/GADR<7>
GADR<8>
GX<11>

FIG.11



61#0
GX<0>
GX<4>
GX<8>
<0>
61#1
GX<1>
GX<4>
GX<8>
<1>
61#2
GX<2>
GX<4>
GX<8>
<2>
61#3
GX<3>
GX<4>
GX<8>
<3>
61#4
GX<3>
GX<5>
GX<8>
<4>
61#5
GX<2>
GX<5>
GX<8>
<5>
61#6
GX<1>
GX<5>
GX<8>
<6>
61#7
GX<0>
GX<5>
GX<8>
<7>
61#8
GX<0>
GX<6>
GX<8>
<8>
61#9
GX<1>
GX<6>
GX<8>
<9>
61#10
GX<2>
GX<6>
GX<8>
<10>
61#11
GX<3>
GX<6>
GX<8>
<11>
61#12
GX<3>
GX<7>
GX<8>
<12>
61#13
GX<2>
GX<7>
GX<8>
<13>
61#14
GX<1>
GX<7>
GX<8>
<14>
61#15
GX<0>
GX<7>
GX<8>
<15>
61#16
GX<0>
GX<7>
GX<9>
<16>
61#17
GX<1>
GX<7>
GX<9>
<17>
61#18
GX<2>
GX<7>
GX<9>
<18>
61#19
GX<3>
GX<7>
GX<9>
<19>
61#20
GX<3>
GX<6>
GX<9>
<20>
61#21
GX<2>
GX<6>
GX<9>
<21>
61#22
GX<1>
GX<6>
GX<9>
<22>
61#23
GX<0>
GX<6>
GX<9>
<23>
61#24
GX<0>
GX<5>
GX<9>
<24>
61#25
GX<1>
GX<5>
GX<9>
<25>
61#26
GX<2>
GX<5>
GX<9>
<26>
61#27
GX<3>
GX<5>
GX<9>
<27>
61#28
GX<3>
GX<4>
GX<9>
<28>
61#29
GX<2>
GX<4>
GX<9>
<29>
61#30
GX<1>
GX<4>
GX<9>
<30>
61#31
GX<0>
GX<4>
GX<9>
<31>

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FIG.12

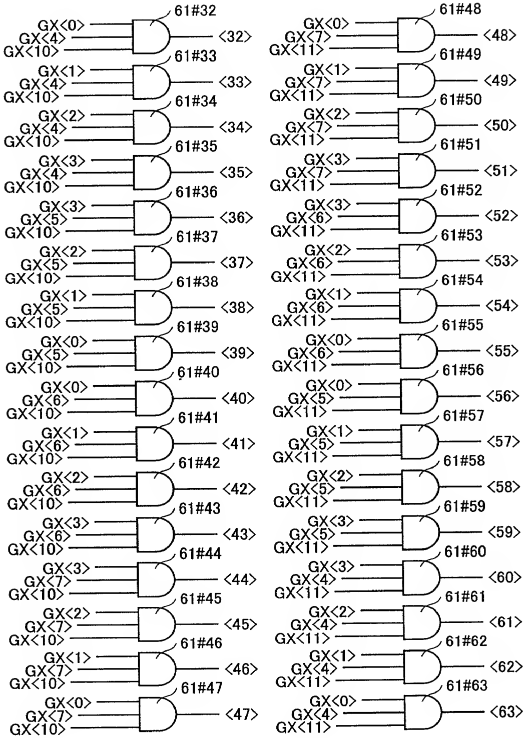
61#32
GX<0>
GX<4>
GX<10>
<32>
61#33
GX<1>
GX<4>
GX<10>
<33>
61#34
GX<2>
GX<4>
GX<10>
<34>
61#35
GX<3>
GX<4>
GX<10>
<35>
61#36
GX<3>
GX<5>
GX<10>
<36>
61#37
GX<2>
GX<5>
GX<10>
<37>
61#38
GX<1>
GX<5>
GX<10>
<38>
61#39
GX<0>
GX<5>
GX<10>
<39>
61#40
GX<0>
GX<6>
GX<10>
<40>
61#41
GX<1>
GX<6>
GX<10>
<41>
61#42
GX<2>
GX<6>
GX<10>
<42>
61#43
GX<3>
GX<6>
GX<10>
<43>
61#44
GX<3>
GX<7>
GX<10>
<44>
61#45
GX<2>
GX<7>
GX<10>
<45>
61#46
GX<1>
GX<7>
GX<10>
<46>
61#47
GX<0>
GX<7>
GX<10>
<47>
61#48
GX<0>
GX<7>
GX<11>
<48>
61#49
GX<1>
GX<7>
GX<11>
<49>
61#50
GX<2>
GX<7>
GX<11>
<50>
61#51
GX<3>
GX<7>
GX<11>
<51>
61#52
GX<3>
GX<6>
GX<11>
<52>
61#53
GX<2>
GX<6>
GX<11>
<53>
61#54
GX<1>
GX<6>
GX<11>
<54>
61#55
GX<0>
GX<6>
GX<11>
<55>
61#56
GX<0>
GX<5>
GX<11>
<56>
61#57
GX<1>
GX<5>
GX<11>
<57>
61#58
GX<2>
GX<5>
GX<11>
<58>
61#59
GX<3>
GX<5>
GX<11>
<59>
61#60
GX<3>
GX<4>
GX<11>
<60>
61#61
GX<2>
GX<4>
GX<11>
<61>
61#62
GX<1>
GX<4>
GX<11>
<62>
61#63
GX<0>
GX<4>
GX<11>
<63>

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FIG.13

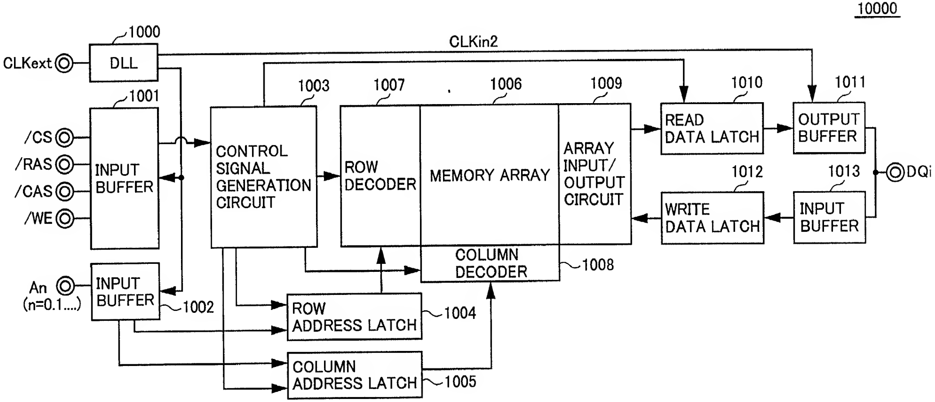
10000
1000
CLKext
DLL
CLKin2
1001
/CS
/RAS
/CAS
/WE
INPUT BUFFER
An (n=0.1....)
INPUT BUFFER
1002
1003
CONTROL SIGNAL GENERATION CIRCUIT
1007
ROW DECODER
1006
MEMORY ARRAY
1009
ARRAY INPUT/ OUTPUT CIRCUIT
COLUMN DECODER
1008
ROW ADDRESS LATCH
1004
COLUMN ADDRESS LATCH
1005
1010
READ DATA LATCH
1011
OUTPUT BUFFER
1012
WRITE DATA LATCH
1013
INPUT BUFFER
DQi

FIG.14

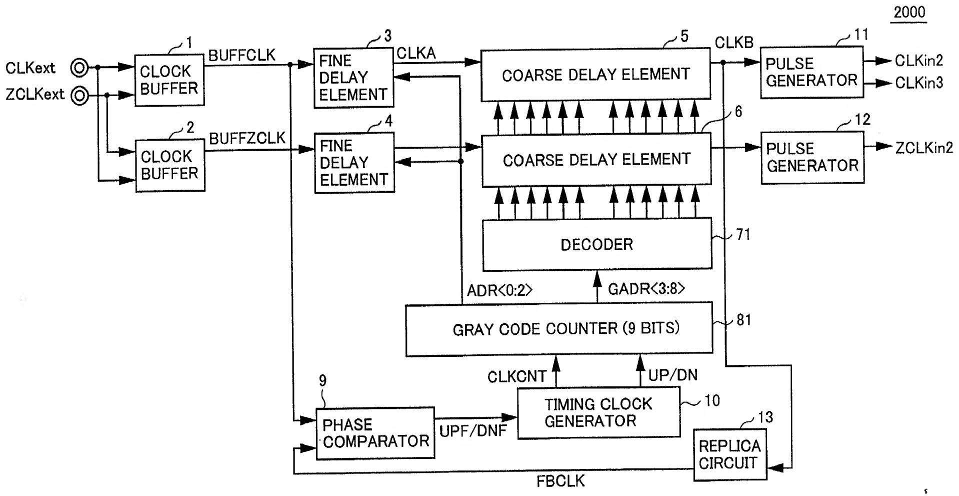
2000
CLKext
ZCLKext
1
CLOCK BUFFER
2
CLOCK BUFFER
BUFFCLK
BUFFZCLK
3
FINE DELAY ELEMENT
4
FINE DELAY ELEMENT
CLKA
5
COARSE DELAY ELEMENT
6
COARSE DELAY ELEMENT
71
DECODER
ADR<0:2>
GADR<3:8>
81
GRAY CODE COUNTER (9 BITS)
CLKCNT
UP/DN
10
TIMING CLOCK GENERATOR
9
PHASE COMPARATOR
UPF/DNF
13
REPLICA CIRCUIT
FBCLK
CLKB
11
PULSE GENERATOR
CLKin2
CLKin3
12
PULSE GENERATOR
ZCLKin2

FIG.15

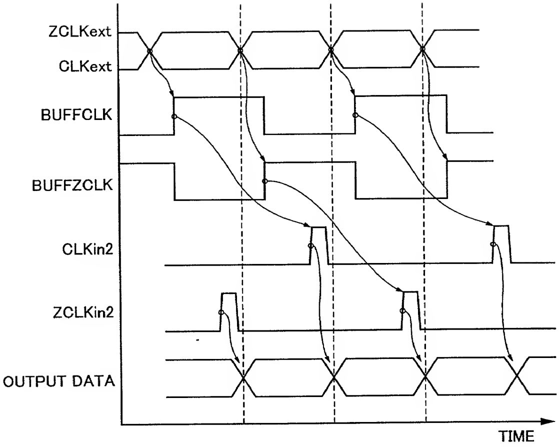
ZCLKext
CLKext
BUFFCLK
BUFFZCLK
CLKin2
ZCLKin2
OUTPUT DATA
TIME

FIG.16

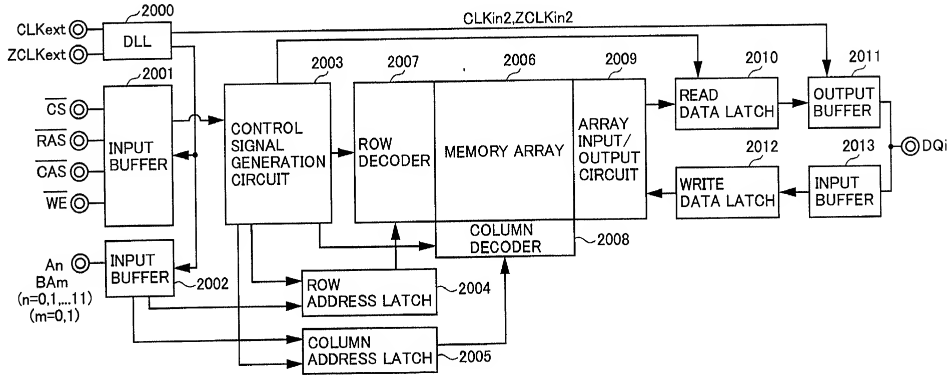
20000
2000
DLL
CLKext
ZCLKext
CLKin2,ZCLKin2
2001
INPUT BUFFER
CS
RAS
CAS
WE
An
BAm
(n=0,1,...11)
(m=0,1)
INPUT BUFFER
2002
2003
CONTROL SIGNAL GENERATION CIRCUIT
2007
ROW DECODER
2006
MEMORY ARRAY
2009
ARRAY INPUT/ OUTPUT CIRCUIT
COLUMN DECODER
2008
ROW ADDRESS LATCH
2004
COLUMN ADDRESS LATCH
2005
2010
READ DATA LATCH
2011
OUTPUT BUFFER
2012
WRITE DATA LATCH
2013
INPUT BUFFER
DQi

FIG.17 PRIOR ART

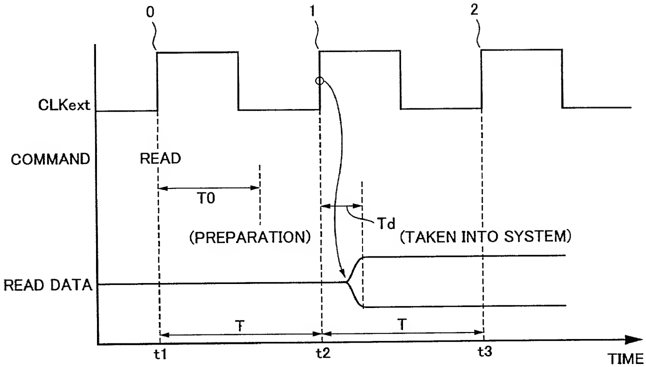
0
1
2
CLKext
COMMAND
READ
T0
(PREPARATION)
Td
(TAKEN INTO SYSTEM)
READ DATA
T
T
t1
t2
t3
TIME

FIG.18 PRIOR ART

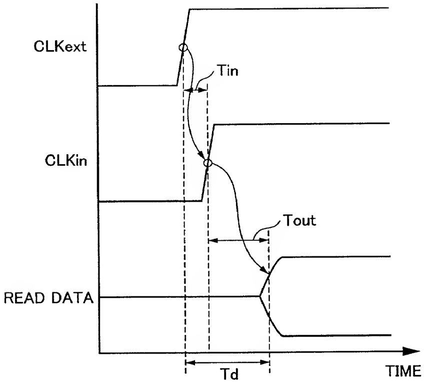
CLKext
Tin
CLKin
Tout
READ DATA
Td
TIME

FIG.19 PRIOR ART

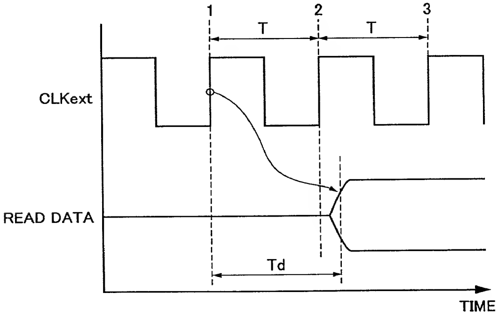
1
2
3
T
T
CLKext
READ DATA
Td
TIME

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FIG.20 PRIOR ART

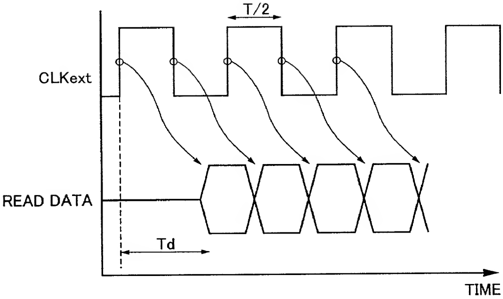
T/2
CLKext
READ DATA
Td
TIME

FIG.21 PRIOR ART

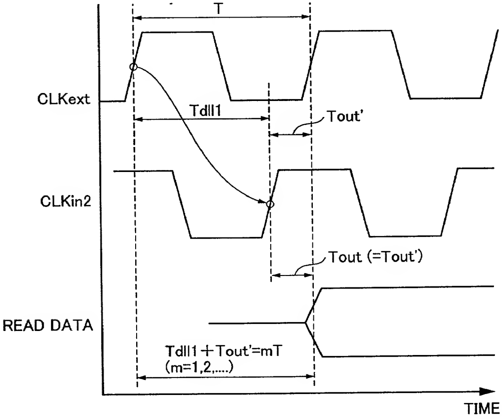
T
CLKext
Tdll1
Tout'
CLKin2
Tout (=Tout')
READ DATA
Tdll1 + Tout'=mT
(m=1,2,.....)
TIME

FIG.22 PRIOR ART

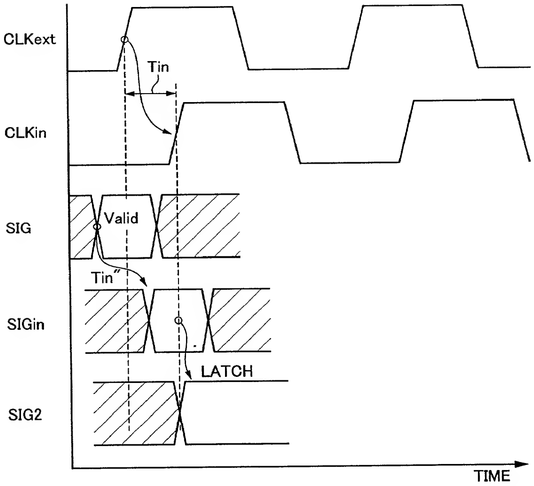
CLKext
Tin
CLKin
SIG
Valid
Tin″
SIGin
LATCH
SIG2
TIME

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FIG.23 PRIOR ART

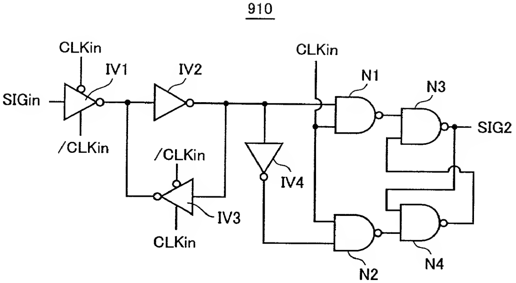

910
CLKin
IV1
IV2
CLKin
N1
N3
SIGin
SIG2
/CLKin
/CLKin
IV4
IV3
CLKin
N2
N4

FIG.24 PRIOR ART

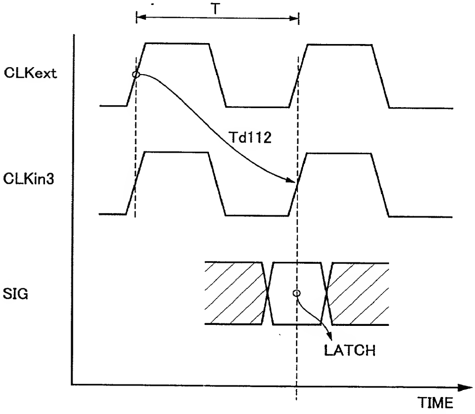

T
CLKext
Td112
CLKin3
SIG
LATCH
TIME

FIG.25 PRIOR ART

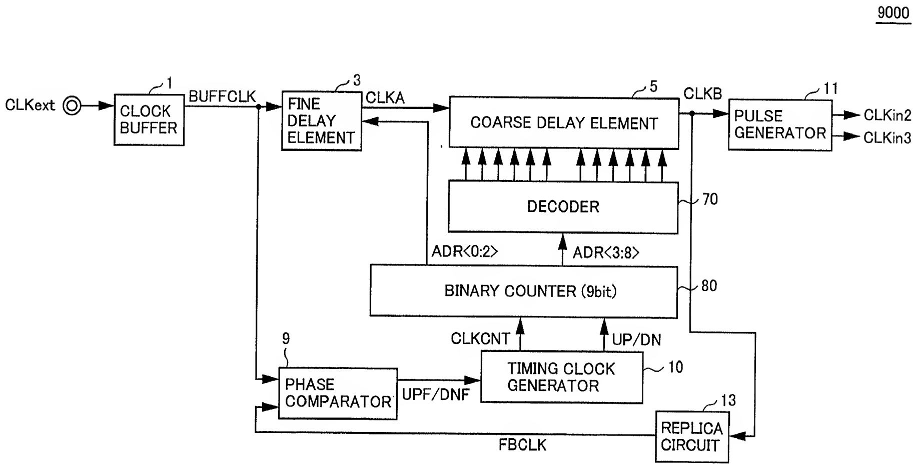

9000
CLKext
1
CLOCK BUFFER
BUFFCLK
3
FINE DELAY ELEMENT
CLKA
5
COARSE DELAY ELEMENT
CLKB
11
PULSE GENERATOR
CLKin2
CLKin3
DECODER
70
ADR<0:2>
ADR<3:8>
BINARY COUNTER (9bit)
80
CLKCNT
UP/DN
9
PHASE COMPARATOR
UPF/DNF
TIMING CLOCK GENERATOR
10
13
REPLICA CIRCUIT
FBCLK

FIG.26 PRIOR ART

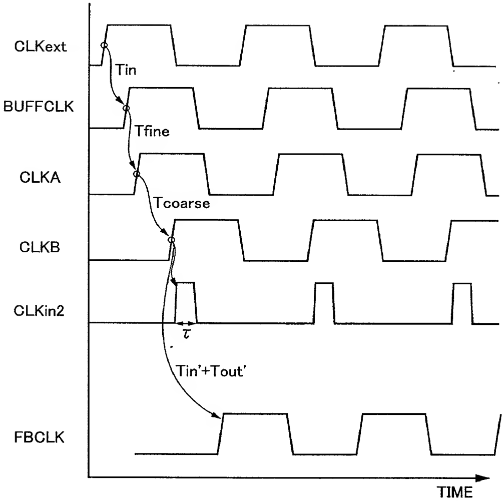

CLKext
Tin
BUFFCLK
Tfine
CLKA
Tcoarse
CLKB
CLKin2
τ
Tin'+Tout'
FBCLK
TIME

FIG.27 PRIOR ART

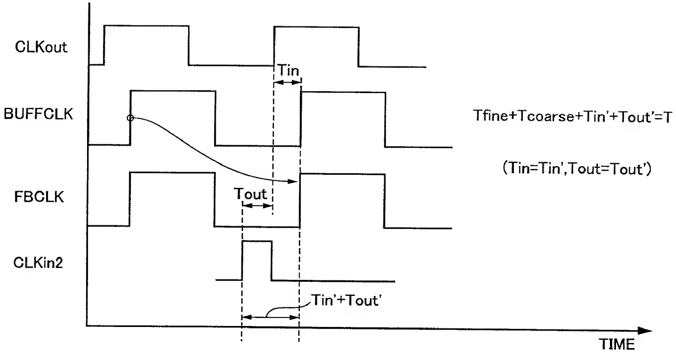

CLKout
Tin
BUFFCLK
Tfine+Tcoarse+Tin'+Tout'=T
(Tin=Tin',Tout=Tout')
FBCLK
Tout
CLKin2
Tin'+Tout'
TIME

FIG.28A PRIOR ART

UP (UPF="H",DNF="L")

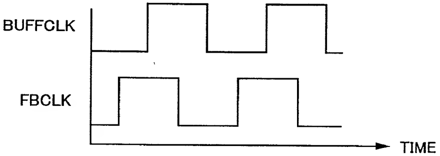
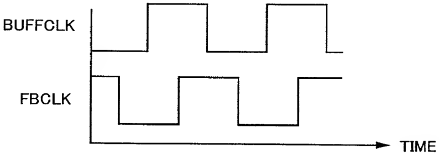

BUFFCLK
FBCLK
TIME

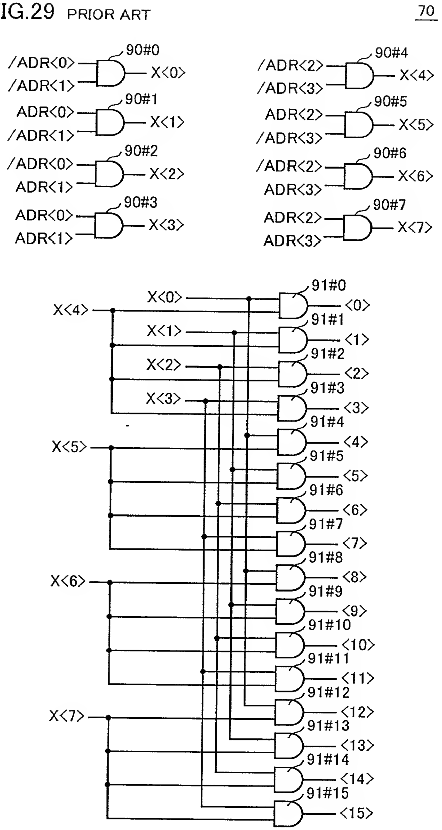
FIG.28B PRIOR ART

DOWN (DNF="H",UPF="L")


BUFFCLK
FBCLK
TIME

10119062 . 072702

FIG.29 PRIOR ART


70
90#0
/ADR<0>
/ADR<1>
X<0>
90#1
ADR<0>
/ADR<1>
X<1>
90#2
/ADR<0>
ADR<1>
X<2>
90#3
ADR<0>
ADR<1>
X<3>
90#4
/ADR<2>
/ADR<3>
X<4>
90#5
ADR<2>
/ADR<3>
X<5>
90#6
/ADR<2>
ADR<3>
X<6>
90#7
ADR<2>
ADR<3>
X<7>
X<4>
X<5>
X<6>
X<7>
X<0>
X<1>
X<2>
X<3>
91#0
<0>
91#1
<1>
91#2
<2>
91#3
<3>
91#4
<4>
91#5
<5>
91#6
<6>
91#7
<7>
91#8
<8>
91#9
<9>
91#10
<10>
91#11
<11>
91#12
<12>
91#13
<13>
91#14
<14>
91#15
<15>

10015706.022702

FIG.30 PRIOR ART

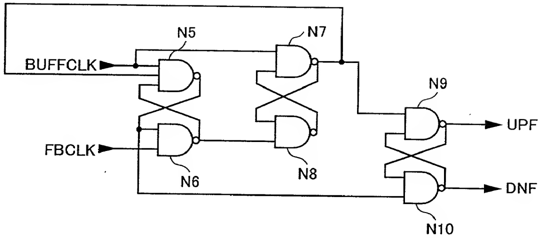

N5
N7
BUFFCLK
N9
UPF
FBCLK
N6
N8
DNF
N10

FIG.31

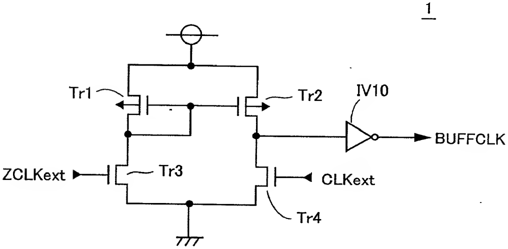
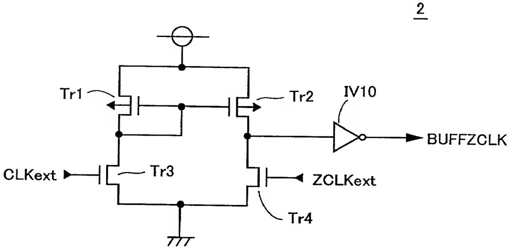

1
Tr1
Tr2
IV10
BUFFCLK
ZCLKext
Tr3
CLKext
Tr4

FIG.32


2
Tr1
Tr2
IV10
BUFFZCLK
CLKext
Tr3
ZCLKext
Tr4

09637027 .083101

FIG.33

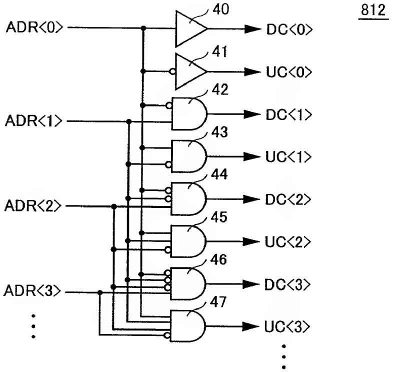
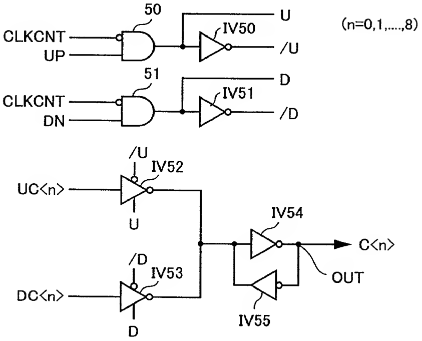

812
ADR<0>
ADR<1>
ADR<2>
ADR<3>
40
41
42
43
44
45
46
47
DC<0>
UC<0>
DC<1>
UC<1>
DC<2>
UC<2>
DC<3>
UC<3>

FIG.34


(n=0,1,....,8)
50
CLKCNT
UP
IV50
U
/U
51
CLKCNT
DN
IV51
D
/D
/U
IV52
UC<n>
U
/D
IV53
DC<n>
D
IV54
C<n>
OUT
IV55